ABSTRACT

A novel method is presented to provide ASICs with drastically reduced NRE and with volume flexibility. The invention includes a method of fabricating an integrated circuit, including the steps of: providing a semiconductor substrate, forming a borderless logic array including a plurality of Area I/Os and also including the step of forming redistribution layer for redistribution at least some of the Area I/Os for the purpose of the device packaging. The fabrication may utilize Direct Write e-Beam for customization. The customization step may include fabricating various types of devices at different volume from the same wafer.

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